

Claims

- [c1] A method for manufacturing a semiconductor device, comprising steps of:
forming source and drain extension regions in an upper surface of a SiGe-based substrate, the source and drain extension regions containing an N type impurity; and
reducing vacancy concentration in the source and drain extension regions to decrease diffusion of the N type impurity contained in the first source and drain regions.
- [c2] The method of claim 1, wherein the step of reducing vacancy concentration comprises a step of providing an interstitial element or a vacancy-trapping element in the source and drain extension regions.
- [c3] The method of claim 2, wherein the interstitial element is Si or O, and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.
- [c4] The method of claim 2, wherein the step of providing the interstitial element or vacancy-trapping element comprises a step of ion-implanting the interstitial element or the vacancy-trapping element onto the SiGe-based substrate.

- [c5] The method of claim 4, wherein the step of ion-implanting the interstitial element or the vacancy trapping element comprises a step of ion-implanting the interstitial element or the vacancy trapping element at an implantation concentration of approximately 1×10^{14} atoms/cm² to 1×10^{16} atoms/cm² and at an implantation energy of approximately 0.3 KeV to 100 KeV.
- [c6] The method of claim 5, wherein the SiGe substrate comprises a Si cap layer on a SiGe film on a silicon substrate.
- [c7] The method of claim 6, wherein a concentration peak of the interstitial element or the vacancy-trapping element and a concentration peak of the N type impurity in the source and drain extension regions are formed at substantially the same depth from an upper surface of the Si cap layer.
- [c8] The method of claim 7, wherein the concentration peak of the interstitial element or the vacancy-trapping element is formed at a depth of approximately 10 Å to 20000 Å from the upper surface of the Si cap layer.
- [c9] The method of claim 4, further comprising a step of annealing.
- [c10] The method of claim 9, wherein the step of annealing is

performed at a temperature of approximately 700°C to 1200 °C for approximately 1 second to 3 minutes.

- [c11] The method of claim 1, further comprising a step of forming a gate electrode on the upper surface of the SiGe-based substrate with a gate oxide film therebetween.
- [c12] The method of claim 1, further comprising a step of forming source and drain regions in the upper surface of the SiGe-based substrate, the source and drain regions containing the N type impurity and overlapping the source and drain extension regions.
- [c13] The method of claim 12, further comprising a step of providing an interstitial element or a vacancy-trapping element in the source and drain regions.
- [c14] The method of claim 13, wherein the interstitial element is Si or O, and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.
- [c15] The method of claim 14, wherein the step of reducing the vacancy concentration in the source and drain regions comprises a step of ion-implanting the interstitial element or the vacancy-trapping element.
- [c16] A method for reducing diffusion of an N type impurity in

a SiGe-based substrate, the method comprising steps of:
forming source and drain extension regions in an upper
surface of the SiGe-based substrate; and
ion implanting an interstitial element or a vacancy-trap-
ping element into the source and drain extension re-
gions to reduce vacancy concentration in the source and
drain extension regions.

[c17] The method of claim 19, wherein the interstitial element
is Si or O, and the vacancy-trapping element is F, N, Xe,
Ar, He, Kr or a noble gas element.

[c18] The method of claim 16, further comprising a step of
forming source and drain regions.

[c19] A semiconductor device comprising:
a SiGe-based substrate;
a gate electrode formed on the SiGe-based substrate
with a gate oxide therebetween;
source and drain extension regions formed in an upper
surface of the SiGe substrate and containing an N type
impurity; and
a low vacancy region formed corresponding to the
source and drain extension regions and containing an
interstitial element or a vacancy-trapping element.

[c20] The semiconductor device of claim 19, wherein the in-

terstitial element is Si or O and the vacancy-trapping element is F, N, Xe, Ar, He, Kr or a noble gas element.